

Fig. 1

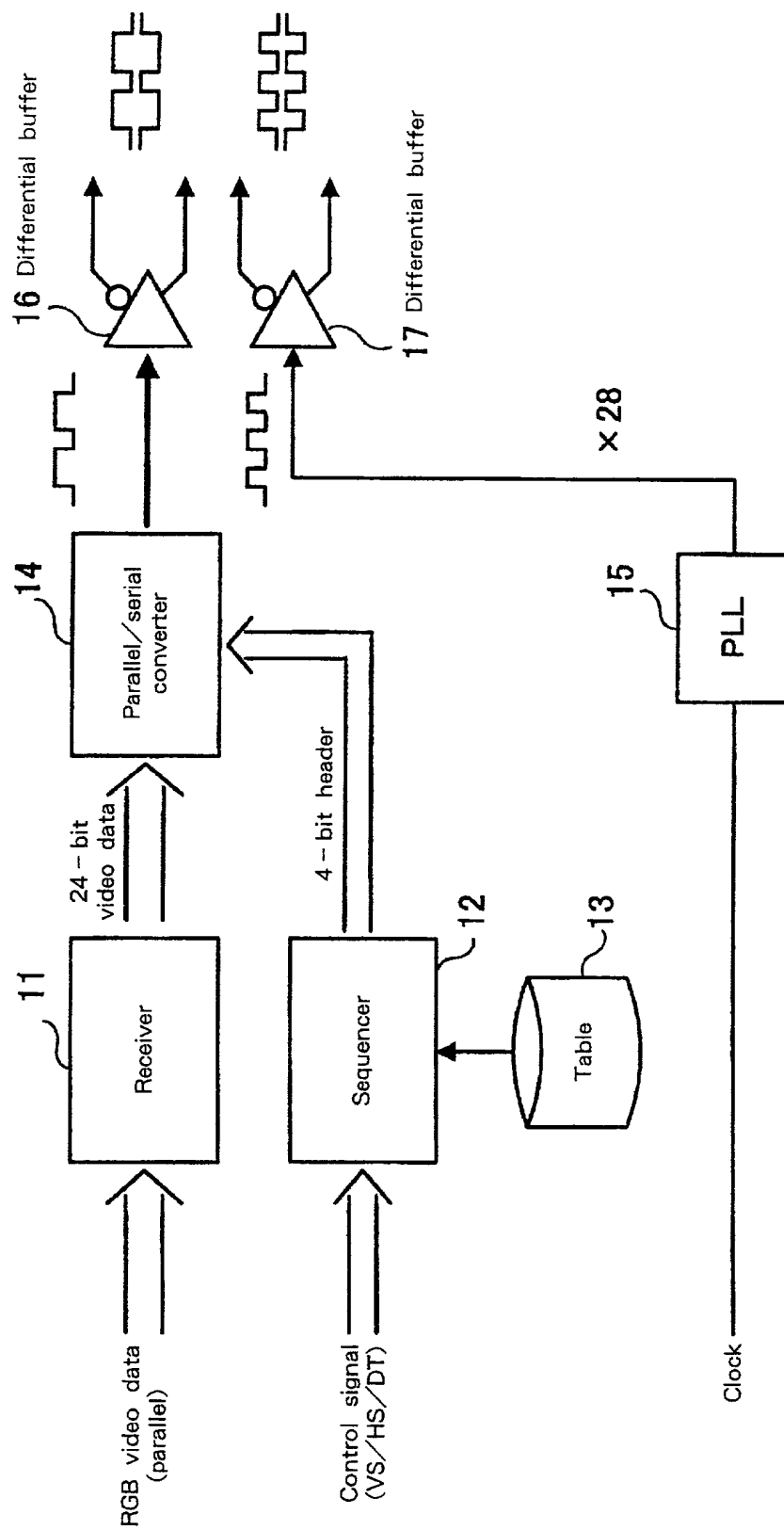


Fig. 2

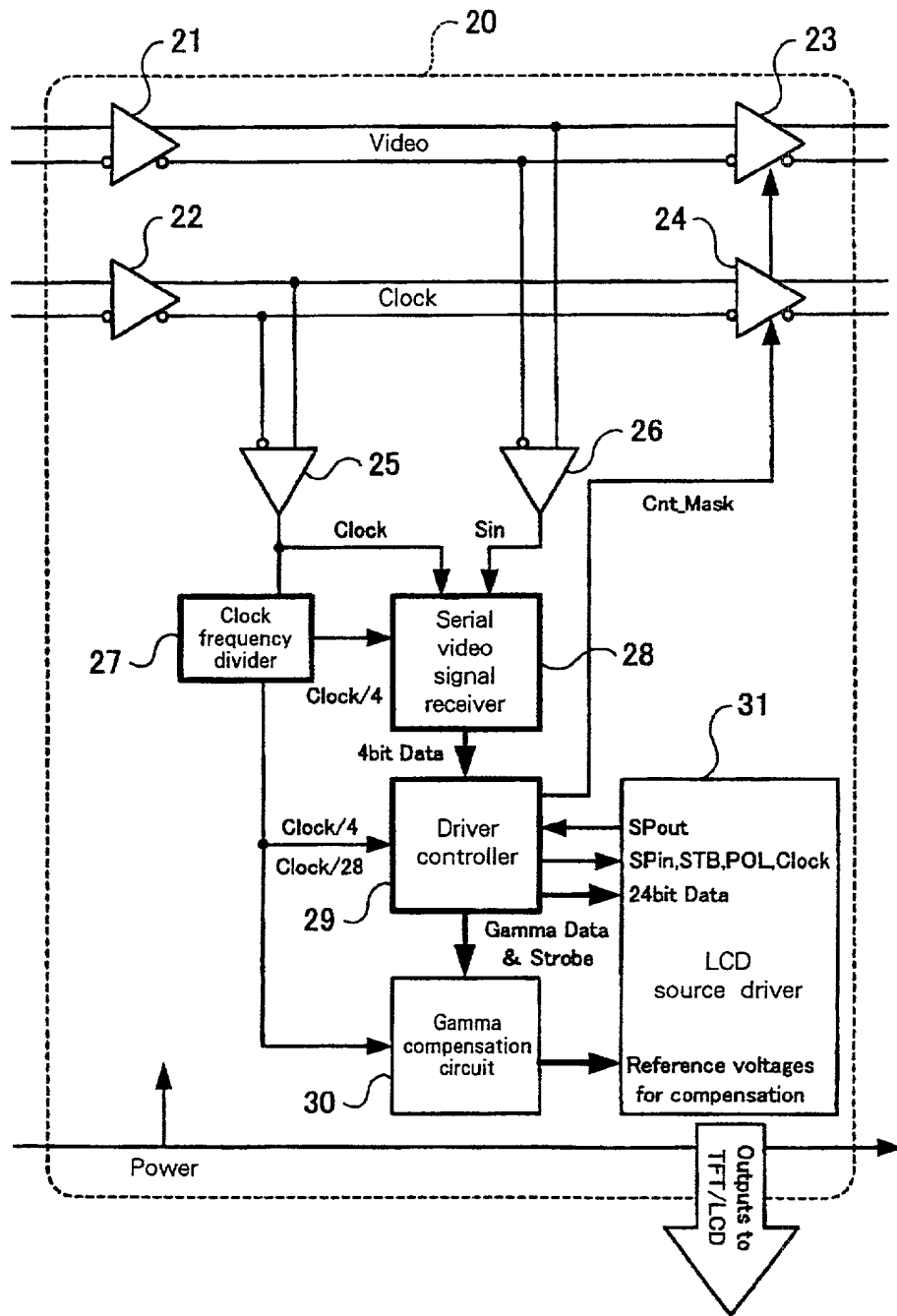


Fig. 3

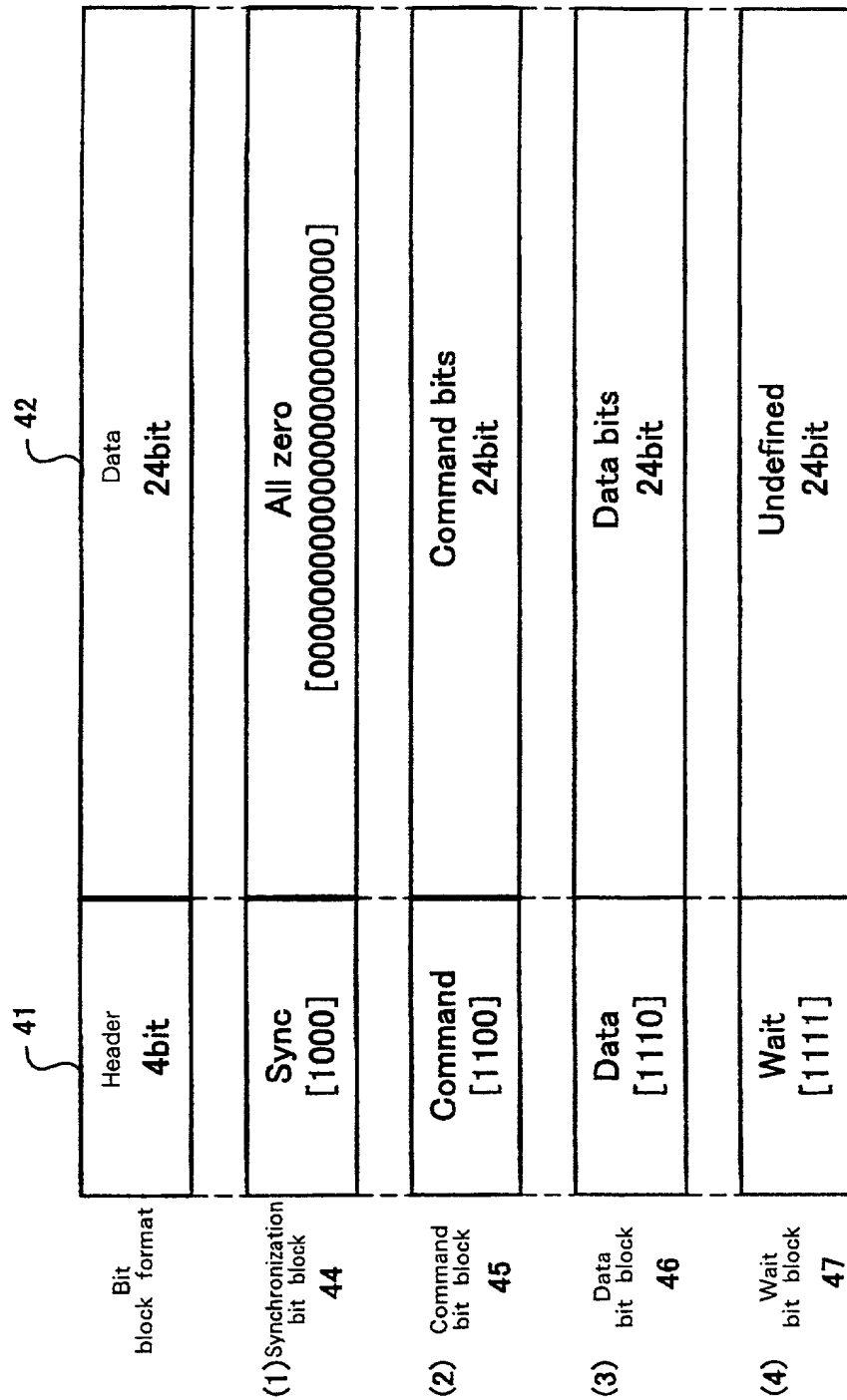


Fig. 4

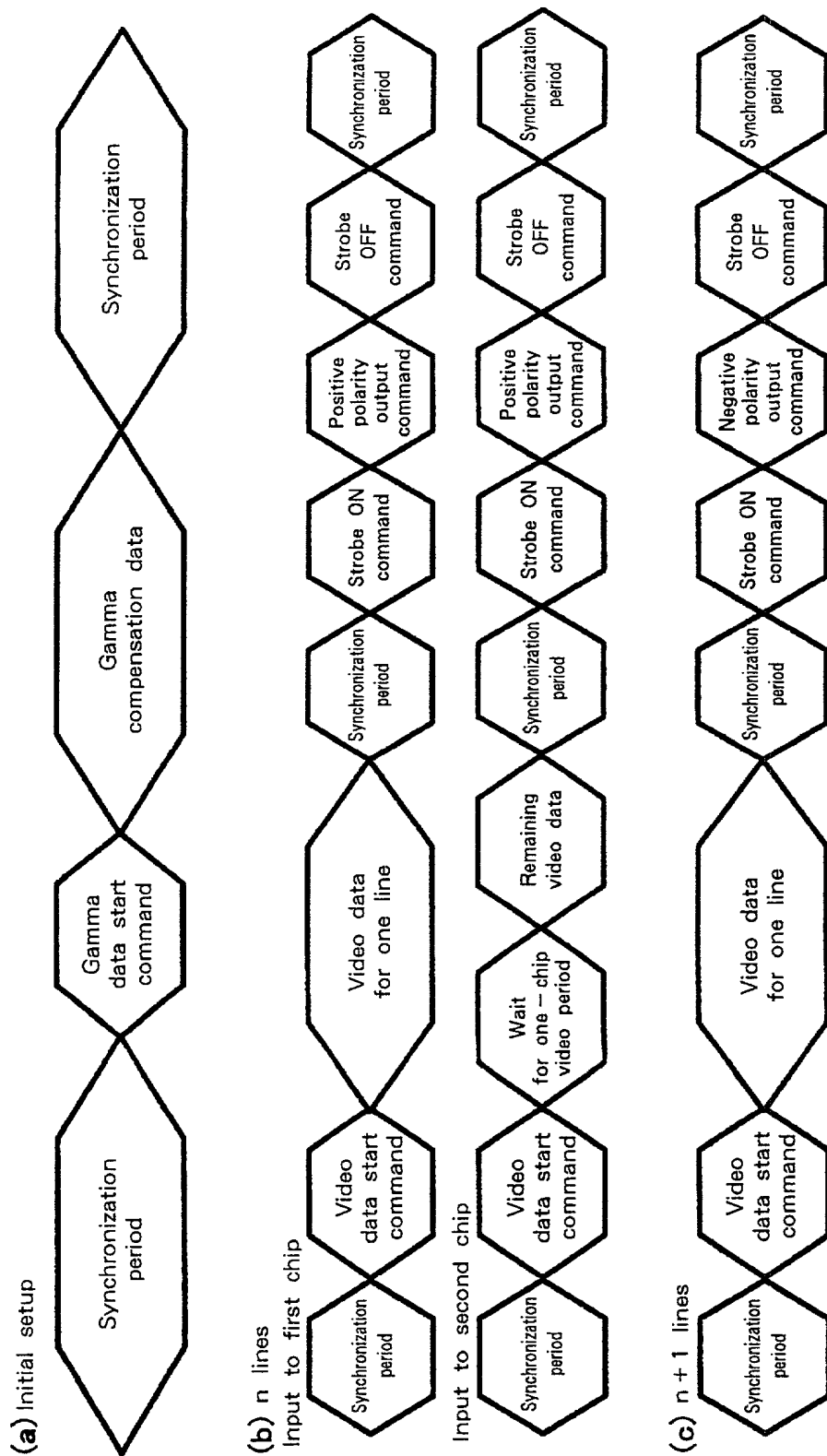


Fig. 5

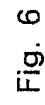


Fig. 6

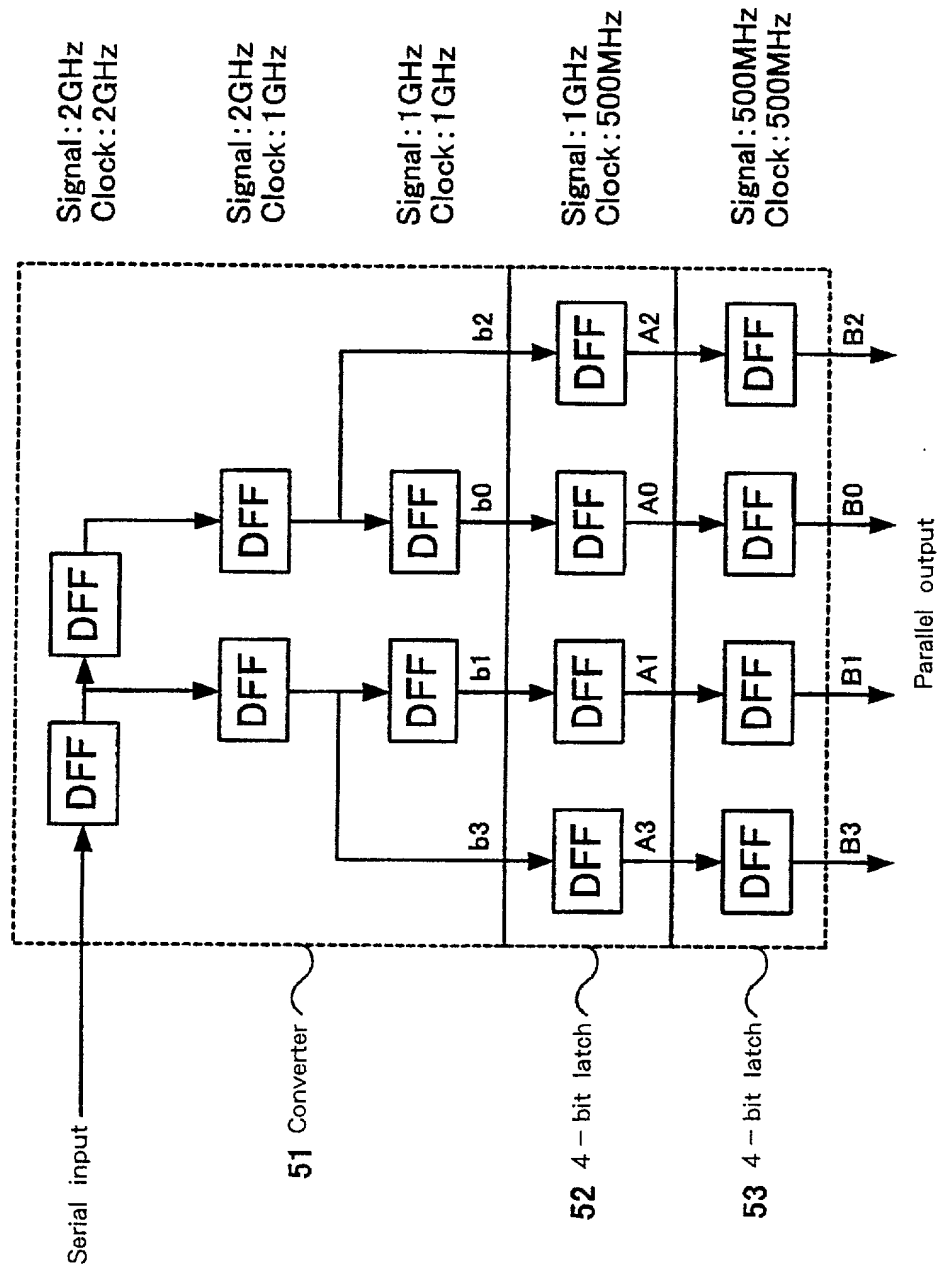


Fig. 7

4 – bit latch (n clock) [A3, A2, A1, A0]	Selector (n + 1 clock) [D3, D2, D1, D0]	Control ID
[1, 0, 0, 0]	[A2, A1, A0, B3]	0
[0, 1, 0, 0]	[A1, A0, B3, B2]	1
[0, 0, 1, 0]	[A0, B3, B2, B1]	2
[0, 0, 0, 1]	[B3, B2, B1, B0]	3

Fig. 8

Bit block type	Comparison pattern with selector output [D3, D2, D1, D0]
Synchronization	[0, 0, 0, 1]
Command	[0, 0, 1, 1]
Data	[0, 1, 1, 1]
Wait	[1, 1, 1, 1]

Fig. 9



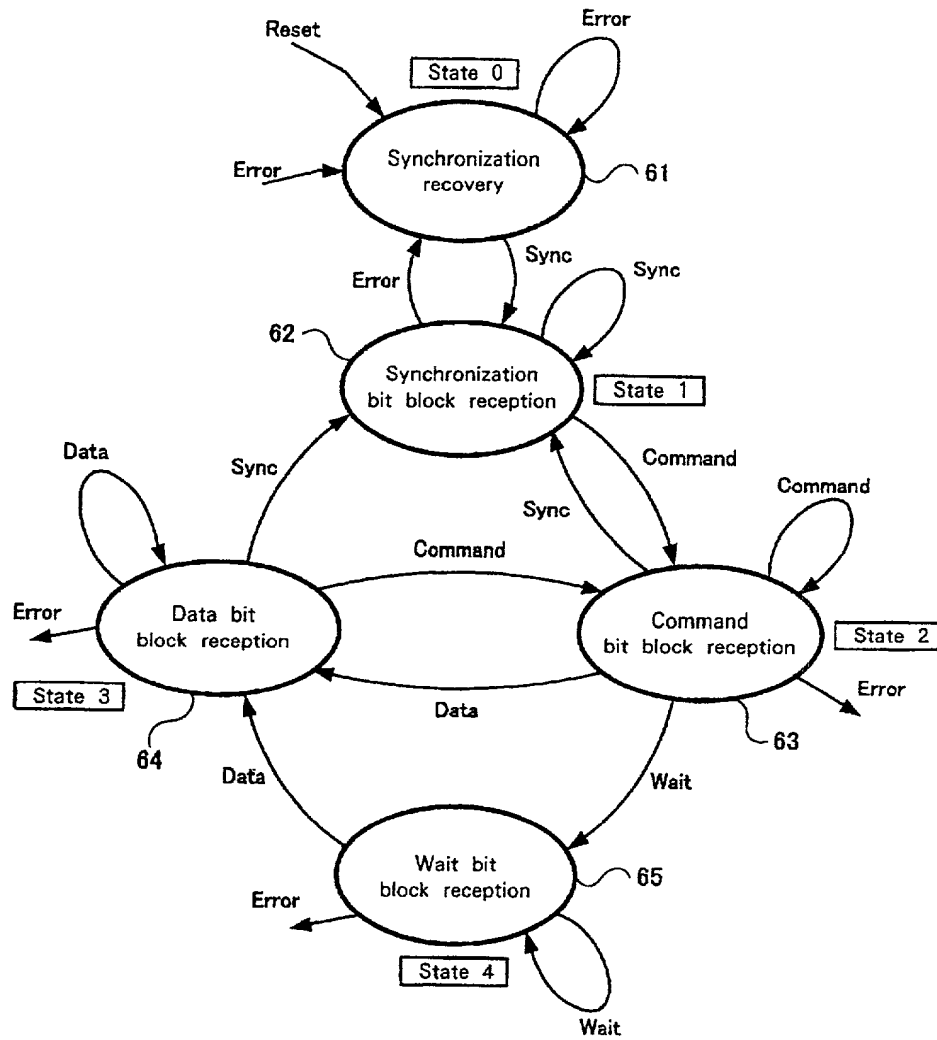


Fig. 10



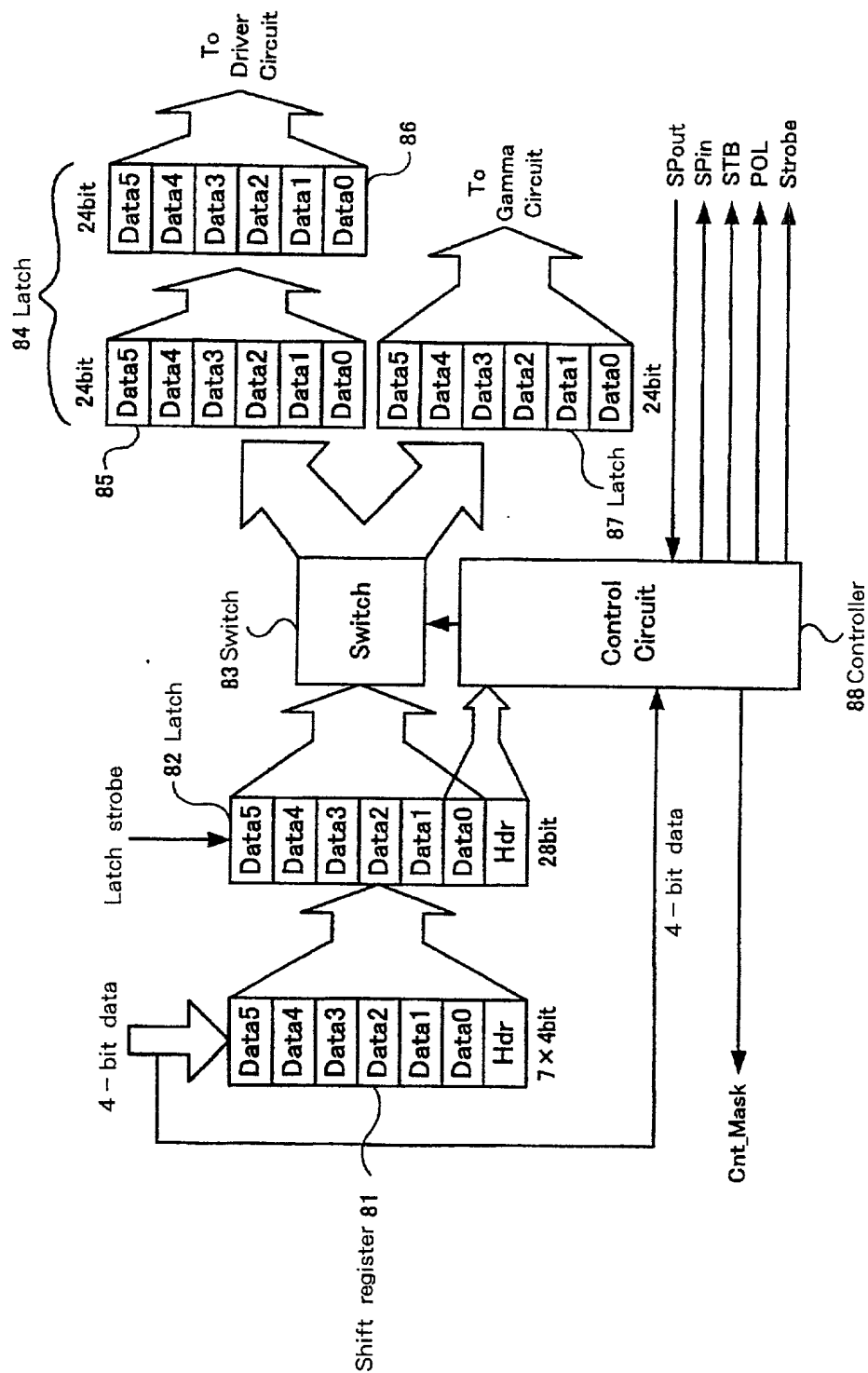


Fig. 12

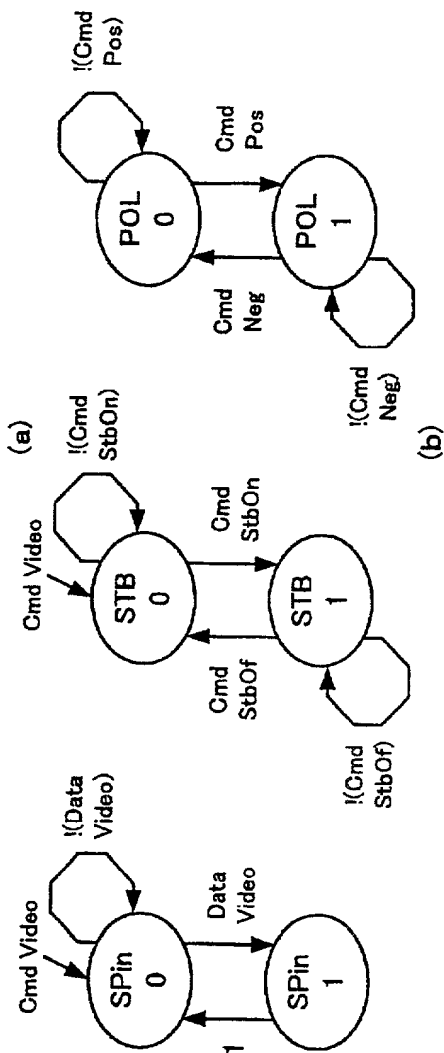
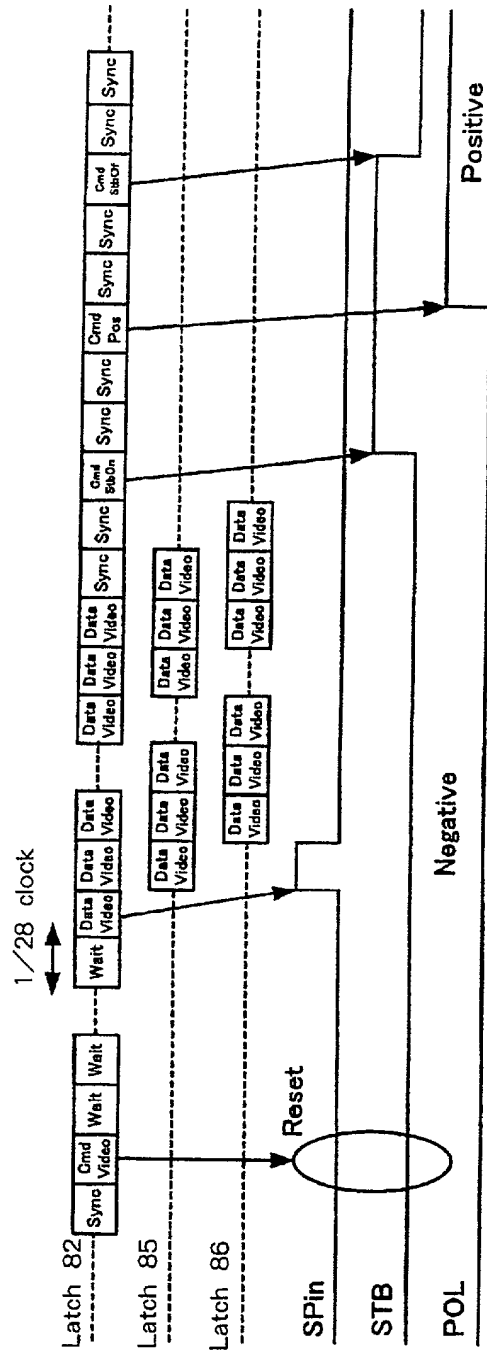


Fig. 13

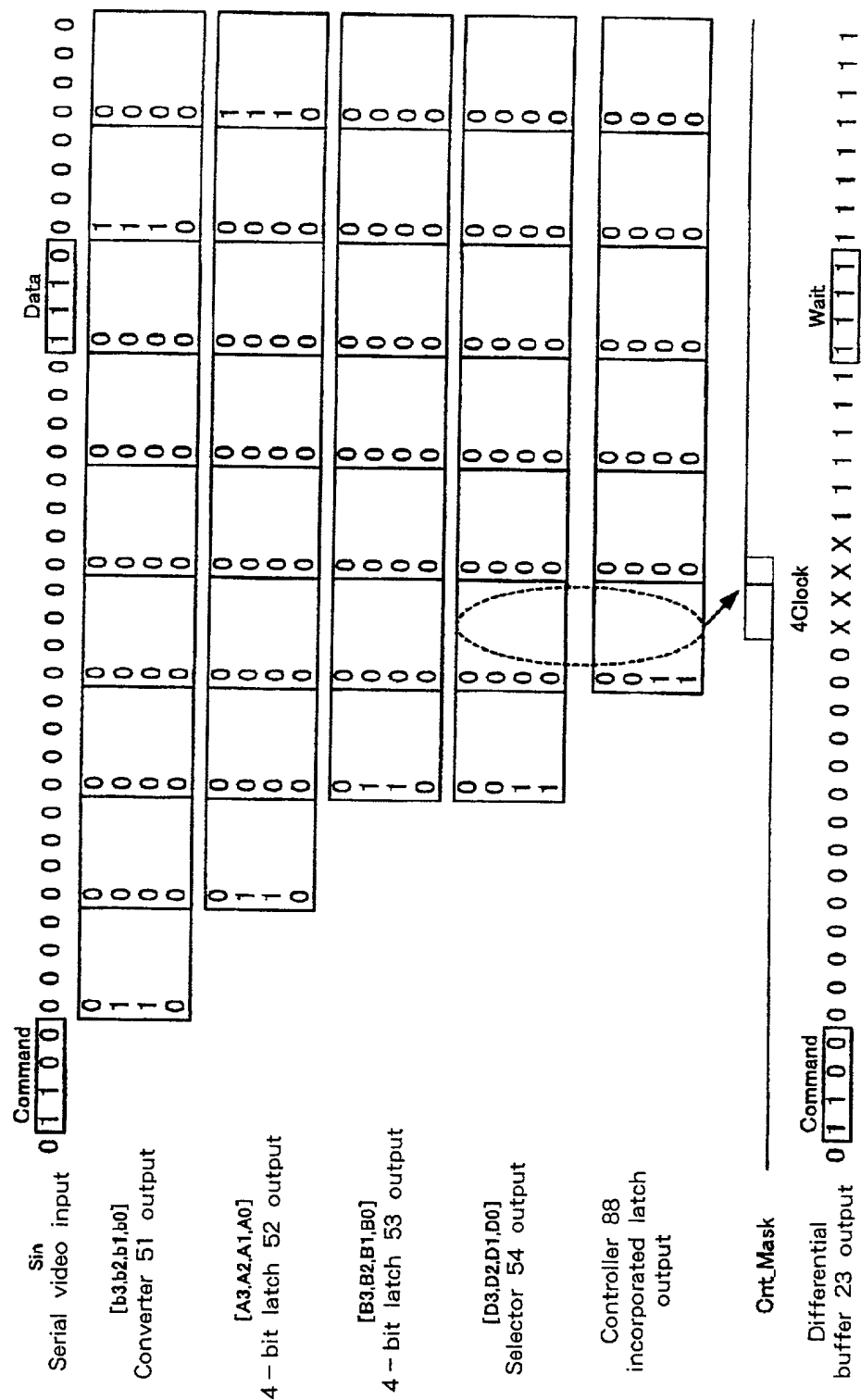


Fig. 14



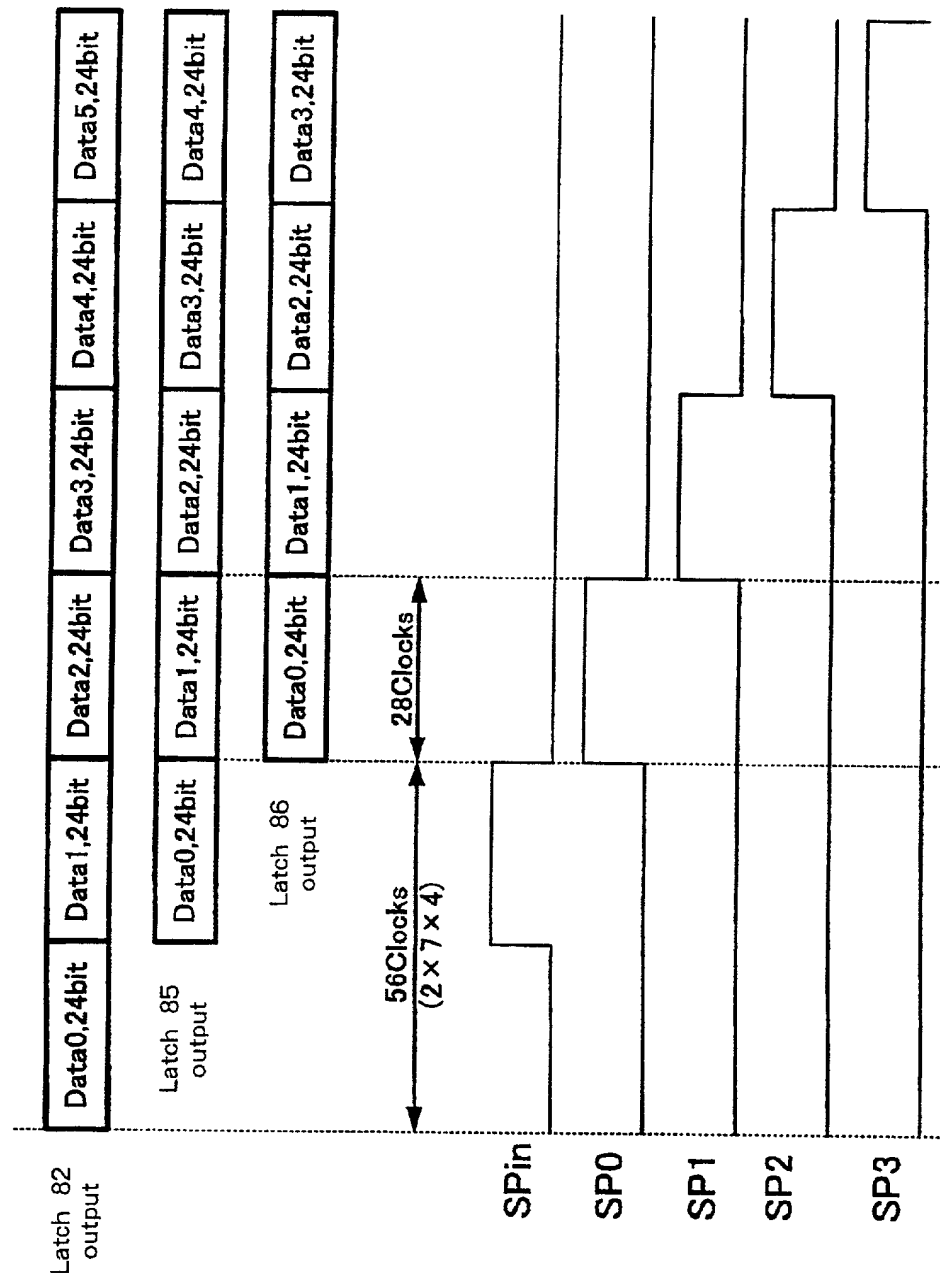


Fig. 16





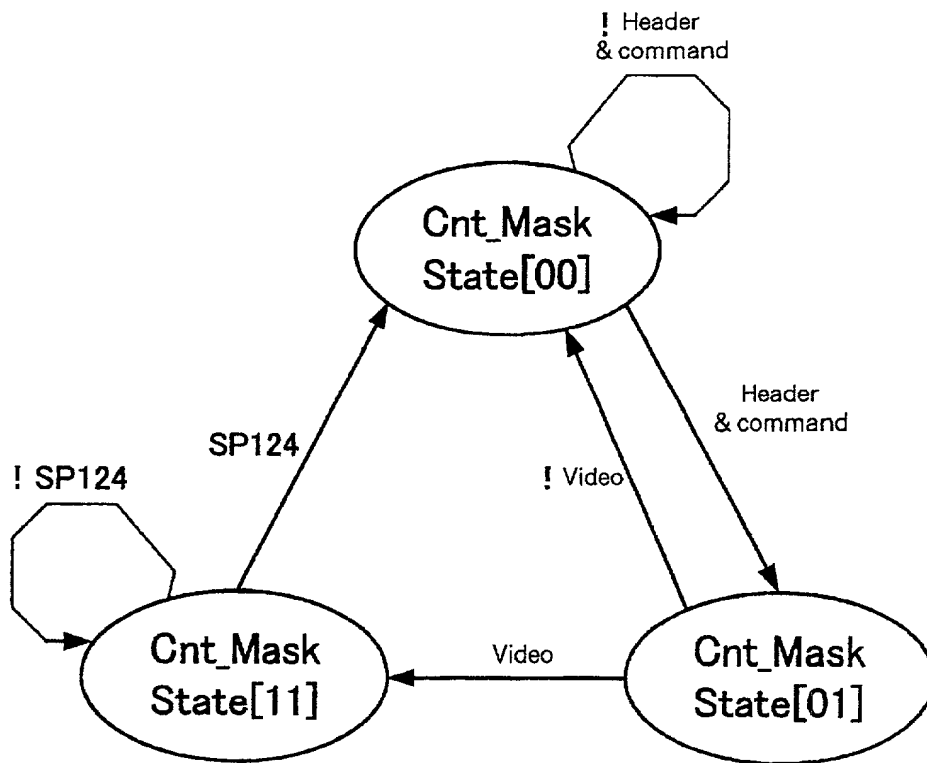


Fig. 18



